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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,139	09/09/2003	Shinji Ohuchi	KKH.039D2	1910

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EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/657,139	OHUCHI ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-37,46 and 53-58* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-37,46 and 53-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/27/07,8/2/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 34-37, 46, 53-56 and 58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (U.S. Pat. 5239198) (previously applied) in view of Okuno et al. (U.S. Pat. 6063646) (newly cited for amended claim 34).

- Regarding claims 34 and 53, Lin et al. (figs. 6-7) disclose a semiconductor device comprising:

a BGA (ball grid array) type semiconductor device including a base plate 12 and a plurality of bumps 32 formed on a backside surface of the base plate; and

a CSP (chip size package) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have the plurality of bumps 32 formed thereon,

the CSP type semiconductor device having a semiconductor element 50 which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals (the plurality of pads or elements 51) which are formed on the main surface,

wherein the back surface and the entirety of the side surfaces of the semiconductor element 50 are exposed;

wherein the backside surface of the base plate is mounted to a printed circuit board 38 via the plurality of bumps, and the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 32 (figs.6- 7, column 6, lines 55 et seq.).

Lin et al. do not disclose a resin that covers the main surface of the semiconductor element and side surface of the terminals.

However, Okuno et al. discloses a CSP type semiconductor device has a resin 4 that covers the main surface of the semiconductor element 1 and side surfaces of the terminals 2 and portion of each of the plurality of terminals are exposed from the resin 4 (fig. 8, abstract). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have a semiconductor element and a resin that covers the main surface of the semiconductor element and side surface of the terminals as taught by Okuno et al. into the device of Lin et al. in order to improve the mounting reliability and achieve a higher production efficiency for the semiconductor package structure.

- Regarding claim 35, Lin et al. disclose that the plurality of terminals of the CSP type semiconductor device are electrically connected to the plurality of bumps 32 (fig. 7) via wiring patterns 16 formed on the backside surface of the base plate (fig. 6, column 6, lines 61-65).
- Regarding claim 36, Lin et al. disclose that the plurality of terminals of the CSP type semiconductor device are coupled to the wiring patterns via solder joint 51 (fig. 7).

- Regarding claim 37, Lin et al. disclose that the CSP type semiconductor device is mounted on the BGA type semiconductor device so that a front surface of the CSP type semiconductor device faces the backside surface of the base plate 12 (fig. 7).
- Regarding claim 46, Lin et al. disclose that the main surface of the semiconductor element 50 faces the backside surface of the base plate 12 (fig. 7).
- Regarding claim 54, Lin et al. disclose that the BGA type semiconductor device has a plurality of conductive portions 42 (fig. 5, column 6, lines 33-34) on the backside surface of the base plate 12, the semiconductor device further comprising a plurality of conductive members 16, each of which is located between a corresponding one of the plurality of conductive portions of a corresponding one of the plurality of terminals (fig. 5).
- Regarding claim 55, Okuno et al. disclose that the plurality of solder balls 3 are not sealed with the resin (fig. 8).
- Regarding claim 56, Lin et al. disclose that the conductive portions 42 are solder (column 6, lines 33-34).
- Regarding claim 58, Lin et al. disclose that the BGA type semiconductor device and the CSP type semiconductor device are individually manufactured.

It is noted that the process limitation: "…the BGA type semiconductor device and the CSP type semiconductor device are individually manufactured…" does not carry weight in a claim drawn to structure.

Initially, and with respect to claims 34 and 58, note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself, *In re Brown,* 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.,* 77 F. 2d 274, 279. 26 USPQ 57, 61 (2d. Cir, 1935).

3. Claims 34, 37, 46, 53 and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inaba et al. (U.S. Pat. 6166443) (previously applied) in view of Okuno et al. (U.S. Pat. 6063646) (previously applied).

- Regarding claims 34 and 53, Inaba et al. disclose a semiconductor device comprising:

a BGA (ball grid array) type semiconductor device including a base plate 22 and a plurality of bumps 28 formed on a backside surface of the base plate; and

a CSP (chip size package) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device which does not have any the plurality of bumps 28 formed thereon,

the CSP type semiconductor device having a semiconductor element 24 which has main and back surfaces, and side surfaces between the main and back surfaces, and a plurality of terminals 27 which are formed on the main surface (fig. 9, column 8, lines 40 et seq.);

wherein the backside surface of the base plate is mounted to a printed board (fig. 8) via the plurality of bumps 8, and the CSP type semiconductor device 24 as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 28 (figs. 8-9).

Inaba et al. do not disclose the back surface and the entirety of the side surfaces of the semiconductor element are exposed.

However, Okuno et al. disclose a semiconductor device comprsising a semiconductor element 1, wherein a back surface and the entirety of the side surfaces of the semiconductor element are exposed; and a resin 4 that covers the main surface of the semiconductor element 1 and side surfaces of the terminals 2 (fig. 8). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of Inaba et al. by having the back surface and the entirety of the side surfaces of the semiconductor element are exposed because as taught by Okuno et al., such exposing the back surface and the entirety of the side surfaces would reduce complexity of implementation of a chip size package (fig. 8).

- Regarding claim 57, Inaba et al. disclose that the BGA type semiconductor device has a semiconductor element 23, a size of the semiconductor element 23 of the BGA type semiconductor device is smaller than a size of the semiconductor element 24 of the CSP type semiconductor device (fig. 9).
- Regarding claim 58, Inaba et al. disclose that the BGA type semiconductor device and the CSP type semiconductor device are individually manufactured (fig. 9). Moreover, The process limitations "said BGA type semiconductor device and said CSP type semiconductor device are individually manufactured", do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Response to Arguments

Applicant's arguments filed 5/30/07 have been fully considered but they are not persuasive.

- The applicant argues that Lin et al. fail to disclose a CSP (chip size packaged) type semiconductor device mounted on an area of the backside surface of the base plate of the BGA type semiconductor device.

The applicant's argument has been fully considered but they are not persuasive because Lin et al. disclose a passive electronic component 50, such as a resistor, diode, decoupling capacitor, or the like mounted on an area of the backside surface of the base plate of the BGA type semiconductor device (figs.6- 7, column 6, lines 55 et seq.). The passive electronic component 50 as taught by Lin et al. is chip size package

type semiconductor device. The chip type semiconductor device would be the passive component (a resistor, a capacitor or a diode).

Furthermore, Okuno et al. discloses a CSP type semiconductor device has a resin 4 that covers the main surface of the semiconductor element 1 and side surfaces of the terminals 2 and portion of each of the plurality of terminals are exposed from the resin 4 (fig. 8, abstract). It would have been obvious to one having ordinary skill in the art to replace the passive electronic component 50 of Lin et al. by a CSP type semiconductor device of the semiconductor element 1 (Okuno et al.). Therefore, Lin et al. in view of Okuno et al. disclose all the limitations as disclose in the independent claims 34 and 53.

- The applicant argues that Lin et al. and Inaba et al. do not disclose the limitations recited in the amended claims 34 and 53, such as: wherein the backside surface of the base plate is mounted to a printed circuit board via the plurality of bumps, and the CSP type semiconductor device as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps.

The applicant's argument has been fully considered but they are not persuasive because Lin et al. clearly disclose the backside surface of the base plate 12 is mounted to a printed circuit board 38 via the plurality of bumps, and the CSP type semiconductor device 50 as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 32 (fig. 7).

Inaba et al. clearly disclose the backside surface of the base plate is mounted to a printed board (fig. 8) via the plurality of bumps 8, and the CSP type semiconductor

device 24 as mounted on the backside surface of the base plate has a thickness less than a thickness of the plurality of bumps 28 (figs. 8-9).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Hoai v Pham/
Primary Examiner, Art Unit 2814

DLN